DEPARTMENT OF
ENGINEERING SCIENCE

A flexible readout circuit for SPAD arrays

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Outline

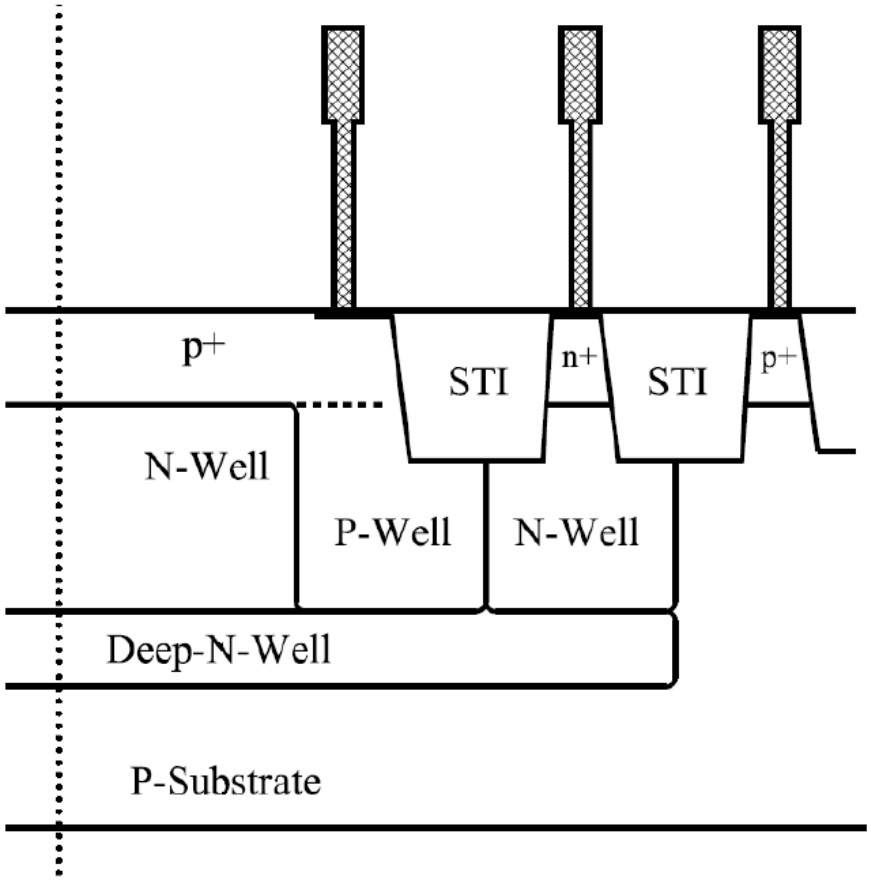
- Photodiode
- SPAD circuit
- 2D array floor plan
- Read-out circuit
- The results in different mode of operation
  - Linear mode
  - Logarithmic mode
  - Dual slope mode

Introduction

- A photodiode is reverse biased and has three main operation mode:
  - Normal: V_R is approximately zero
  - APD: V_R high but smaller than the breakdown voltage
  - SPAD: V_R is above the breakdown voltage (Geiger mode)
- The over-voltage is the difference between the applied and the breakdown voltages
- Photon counting is used to measure the intensity of the incident light by counting the number of detected photon in a specific time interval

The Photodiode

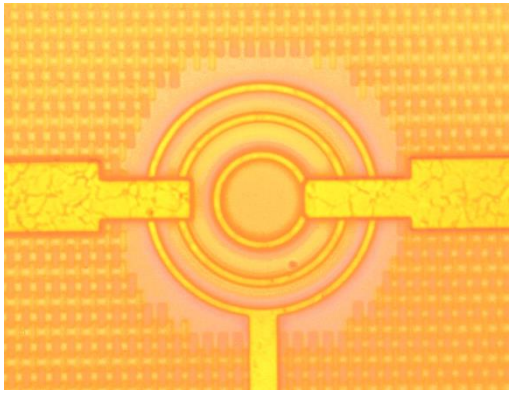
- The active junction is P+/N-Well
- To avoid premature breakdown we need to reduce high electrical field at junction edges and corners
- To avoid corners the photodiode is circular
- A P-Well guard ring reduces the doping concentration and hence electrical field

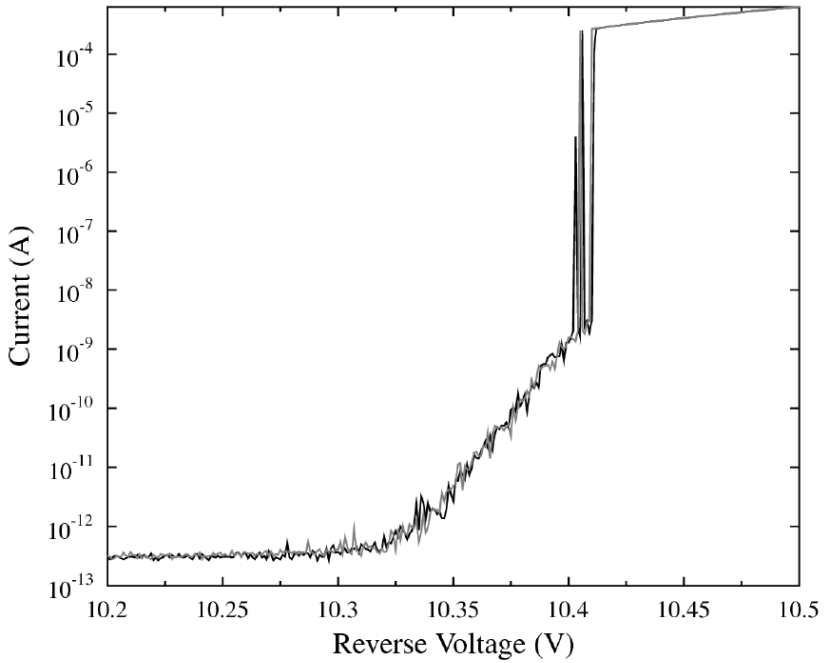


Radial cross section

The Photodiode

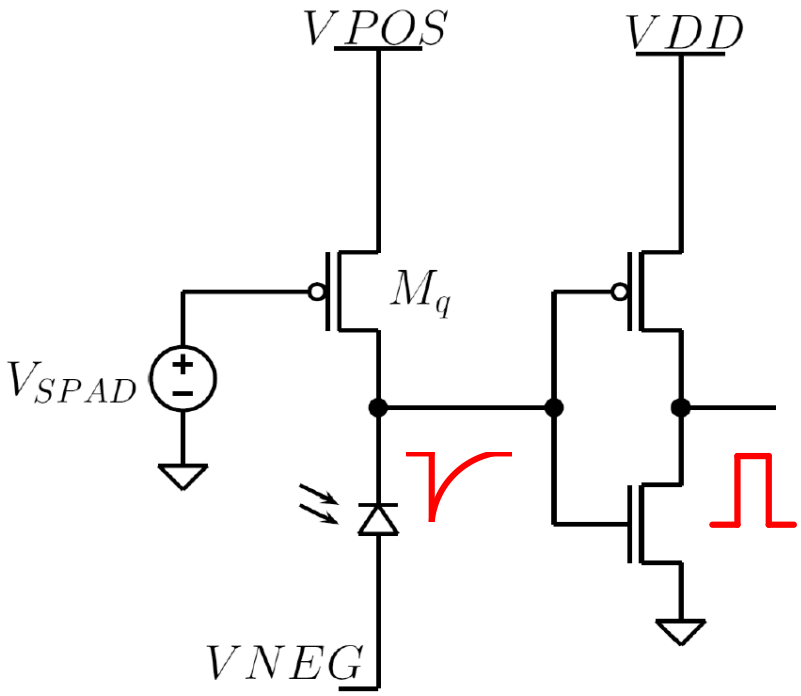
- Fabricated in a UMC CMOS 0.18 µm 1P6M triple-well (Deep-Nwell)
- Silicide is removed to improve the QE
- Results show that the breakdown voltage for these devices is 10.4 V





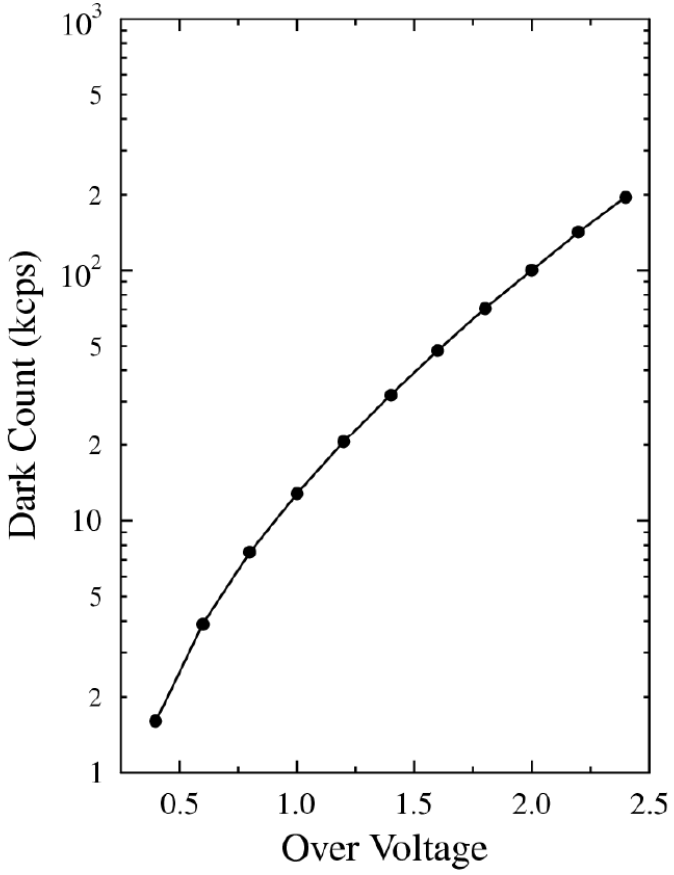
The SPAD circuit

- This circuit generates short pulses when a photon induces and avalanche event
- When an avalanche occurs the SPAD node is discharged
- Current source Mq has two roles:
  - limits the current to quench the SPAD
  - then recharges the SPAD node to its initial state
- Timing is controlled by V_{SPAD}
- Inverter serves two purpose:
  - sharpens up the output pulses
  - acts as an output buffer



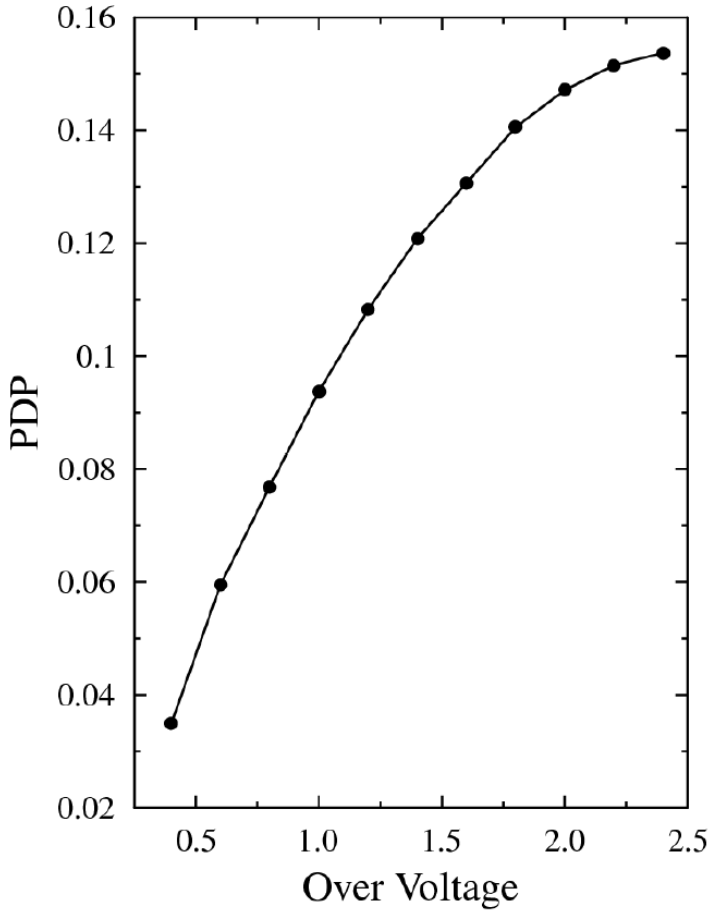
Dark Count Rate

- The pulse count rate in the absence of light
- Contributing factors include:
  - Generation-recombination
  - Charge Traps
  - Tunnelling noise
- These mechanisms mean that the DCR increases with over-voltage



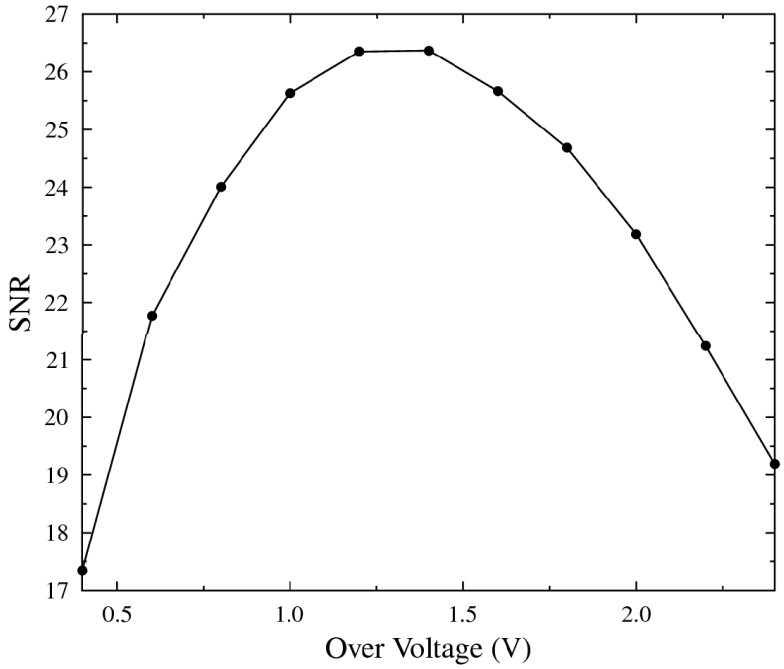
Photon Detection Probability

- The ratio of number of pulses to the expected number of incident photons
- Product of QE and avalanche probability
- Increases with over voltage
- Has a saturation limit
- Limit is 16% when measured using green LED (λ=570nm)



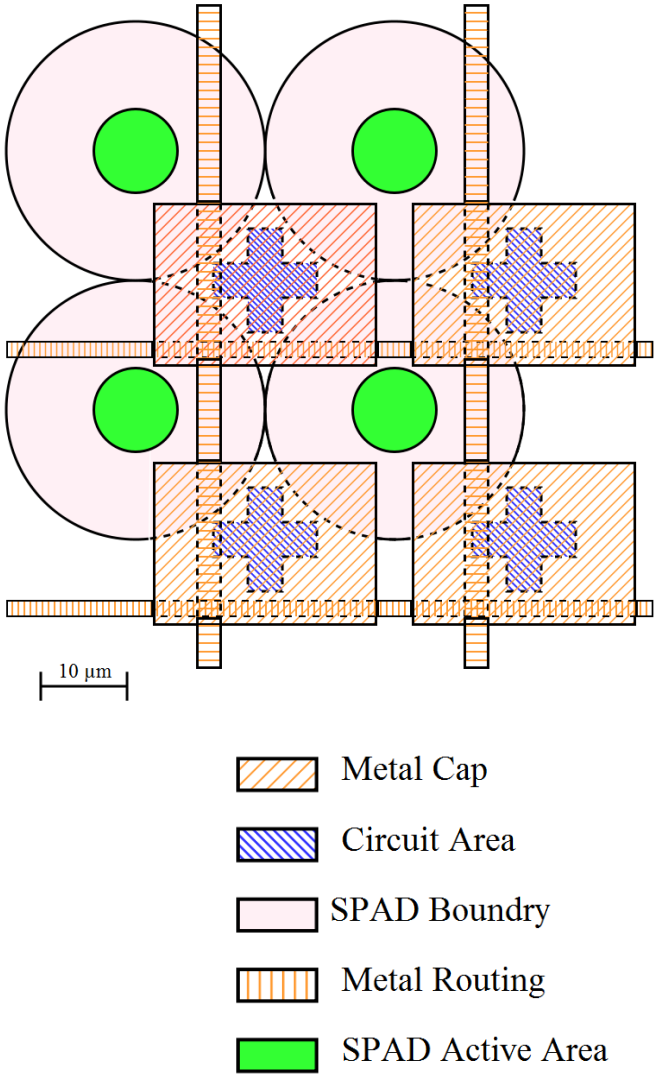
Optimum Overvoltage

- DCR and PDP both increase with overvoltage but at different rates
- If Vex is small, PDP is too low
  If Vex is large, DCR is too high
- SNR=μ/σ (@ 1.1 lux in 16ms)
  - μ: Average Number of events in integration time with average DCR deducted
  - σ: Overall photon shot noise and DCR shot noise
- Optimum Vex for this device is approximately 1.25V
- Experiments were performed with a Vex of 1.0V



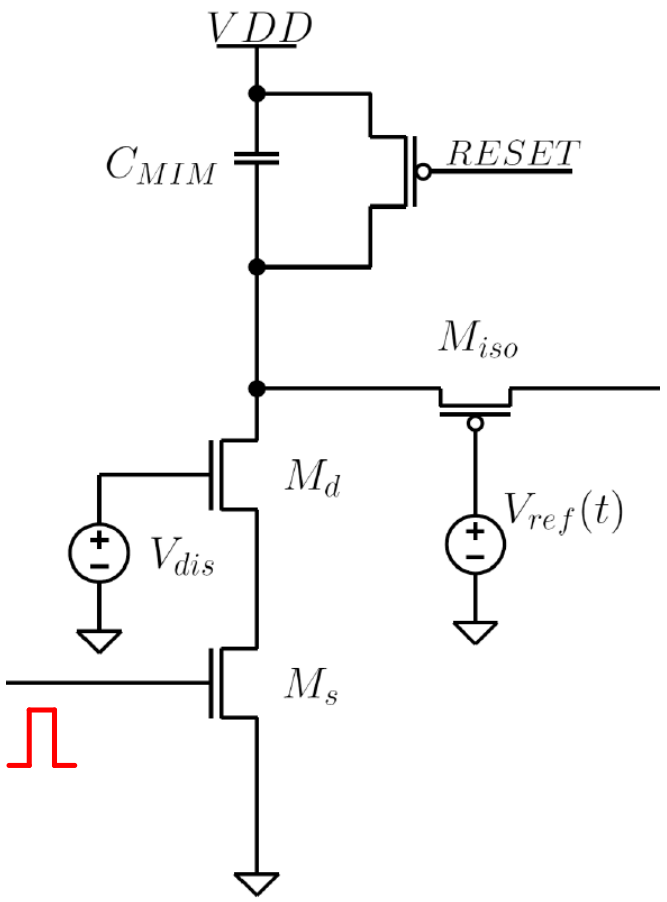
Floor Plan for a 2D Array

- Floor plan for maximum density using the SPAD layout described by Andreou [2007]
- The available area between each SPAD is used to implement the read-out circuit
- A digital counter is too large to fit into this space
- An analogue circuit is designed to fit into this area
- For convenience the read-out circuit is similar to conventional pixels



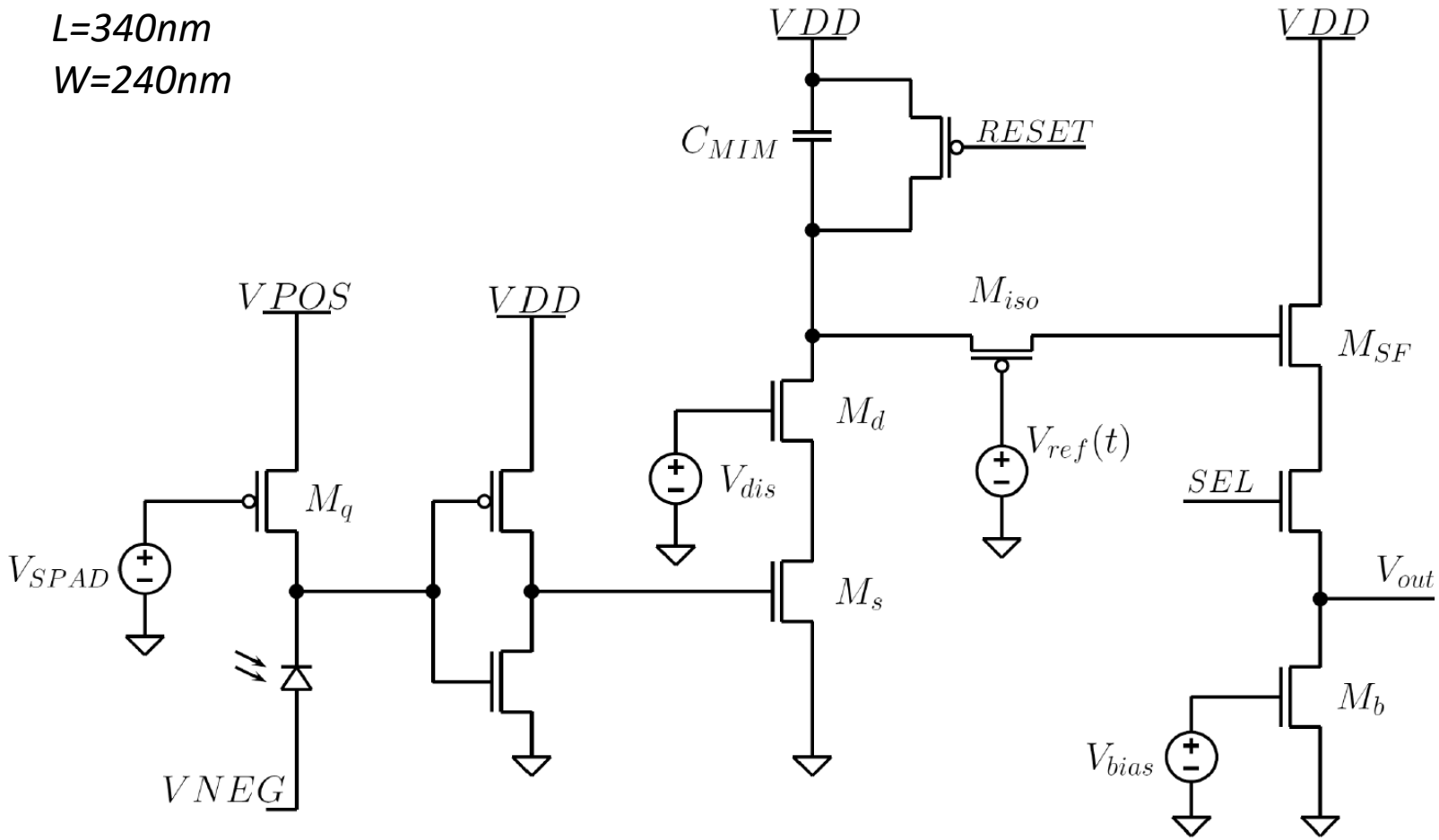
The Pixel

- This circuit stores the number of counts in form of an analogue voltage
- At the beginning of each integration time, capacitor C_{MIM} is reset to VDD
- Ms is an NMOS switch which allows C_{MIM} to be discharged for a short period of time per pulse
- Md is a current source which limits the discharge current
- M_{iso} is the isolation PMOS device. Its gate voltage is hold to zero for linear mode of operation
- A source follower is used for readout

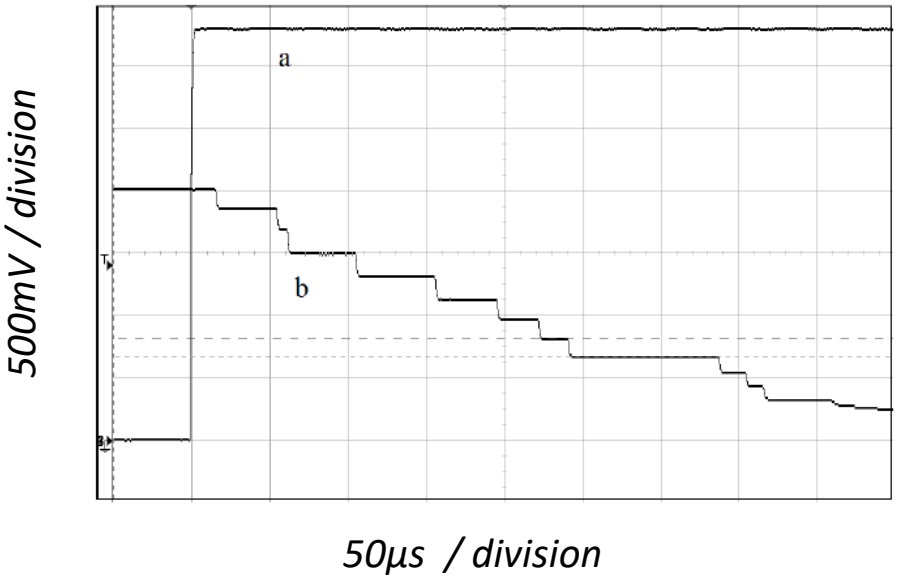


The Overall Pixel Circuit

L=340nm
W=240nm



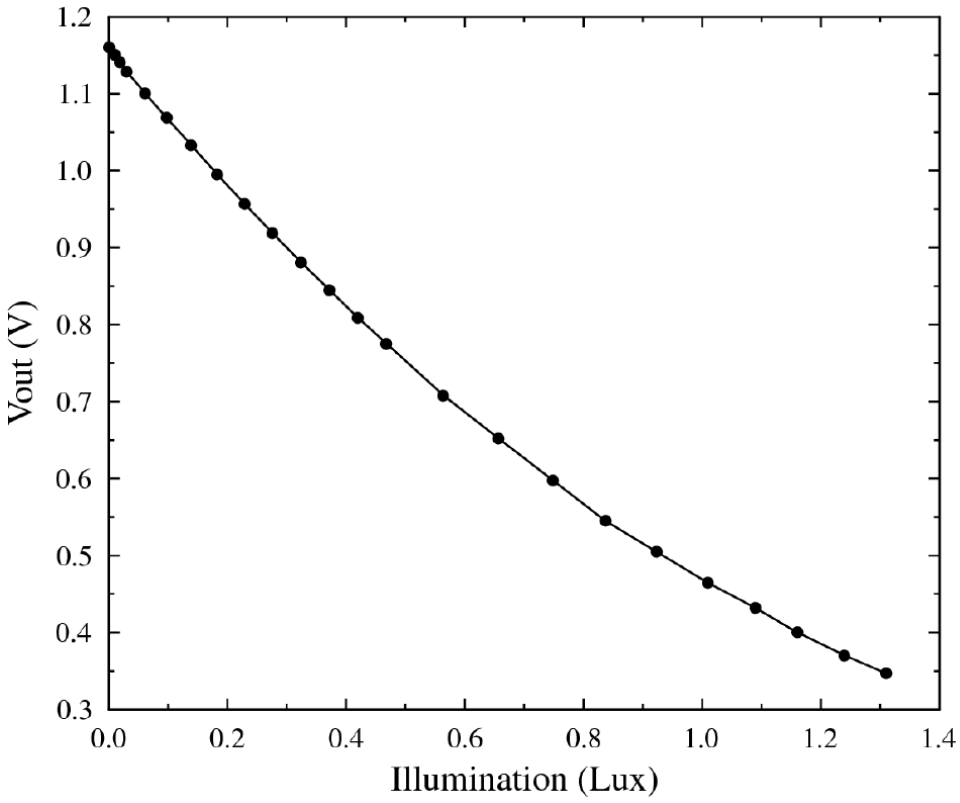
The Results (Linear)



- Discharging of capacitor in linear mode
  - a: reset pulse
  - b:output voltage
- For clarity each step is approximately 140mV
- Starts from 2.0V: about 1V lost due to source follower
- End at 0.3V: minimum output of the source follower

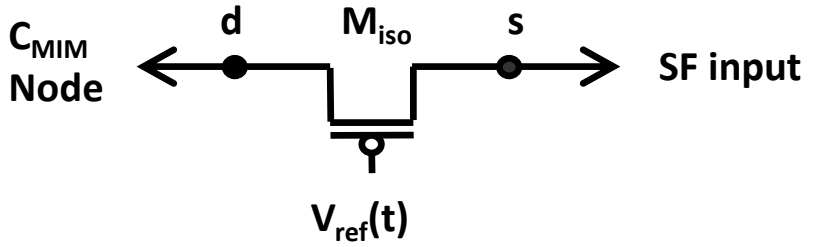
The Results (Linear)

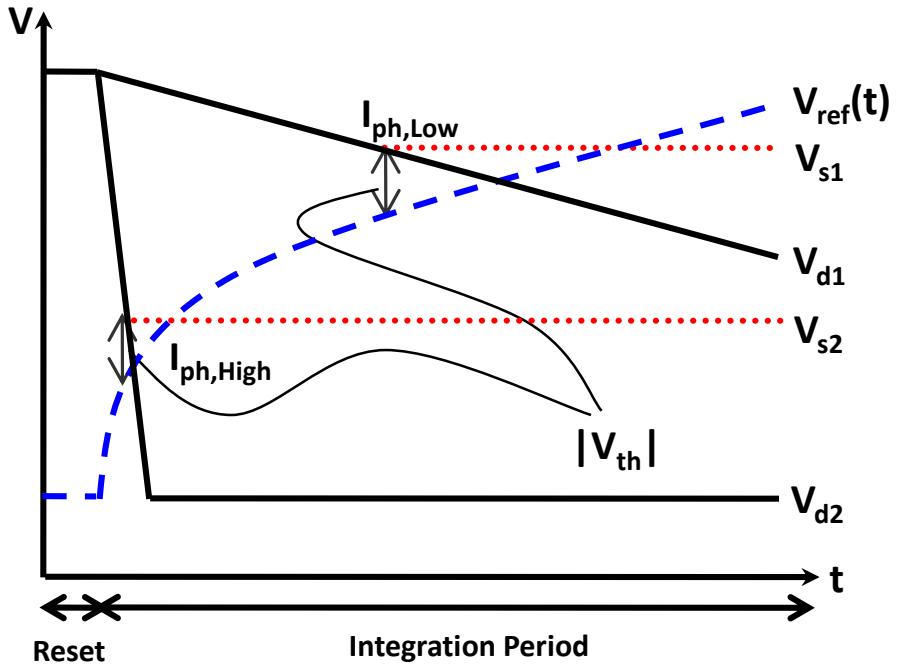
- Each photon caused a change in output voltage of 2mV.
- Dark count rate means that the voltage changes even in the dark
- The observed deviation for the ideal linear response is due to gate length modulation in the minimum length Md
- Can be corrected by making Md longer or by using a cascode device



Isolation Mode

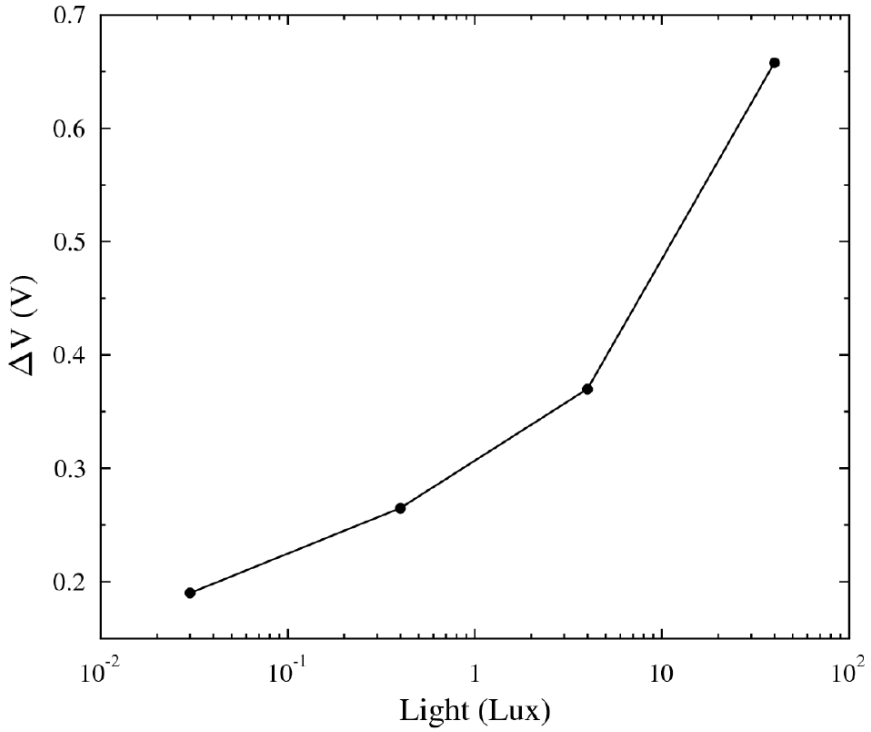
- M_{iso} can be used to isolate the C_{MIM} node from source follower input
- M_{iso} turns off when $|V_{gs}| < |V_{th}|$
- In this case, when $V_{C_{MIM}} - V_{ref}(t) < |V_{th}|$
- $V_{ref}(t)$ can be used by the user to control the pixel response
  - previously used to obtain a logarithmic response in a conventional CMOS pixel



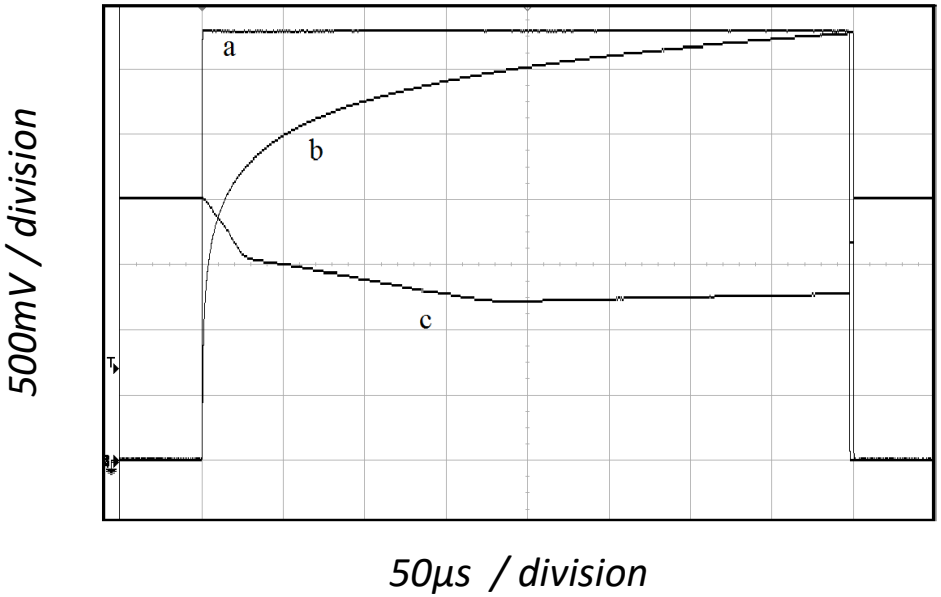


The Pixel Response Results

- Initial tests using the $V_{ref}(t)$ previously used to obtain a logarithmic response with a conventional CMOS pixel
- $V_{ref}(t)$ is not optimised for this pixel
- As expected this results in a high dynamic range in a small voltage range
- However not the expected logarithmic response

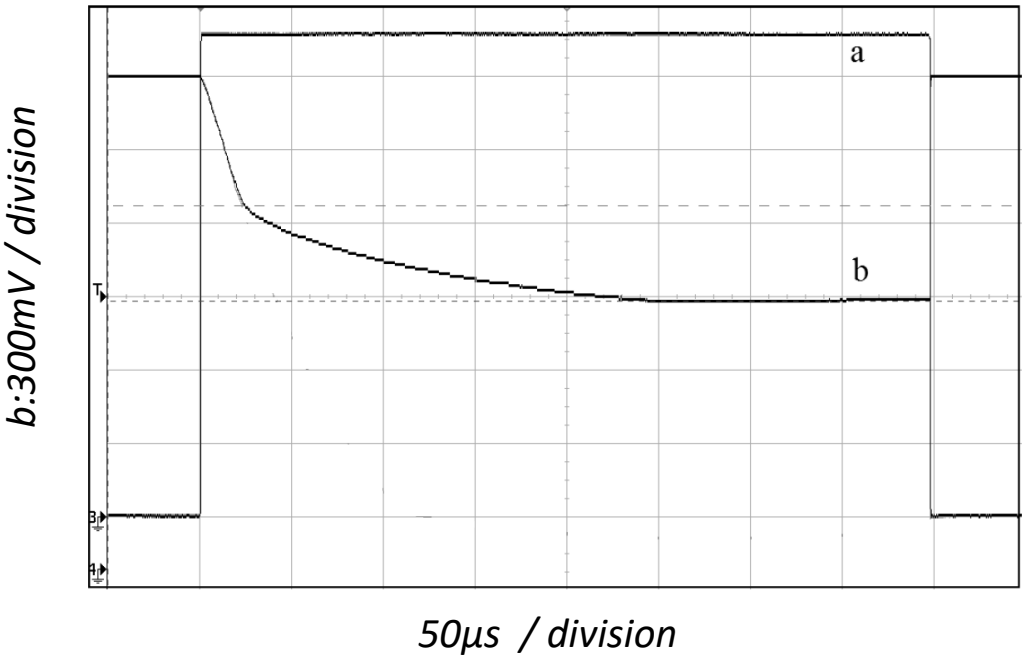


Pixel Time Dependence



- Observe the operation of a pixel
  - a: reset pulse
  - b: $V_{ref}(t)$
  - c: pixel output
- Initial rapid change in pixel voltage during first ms as expected
- Rather than be isolated the voltage continues to change with a lower slope until it becomes almost constant

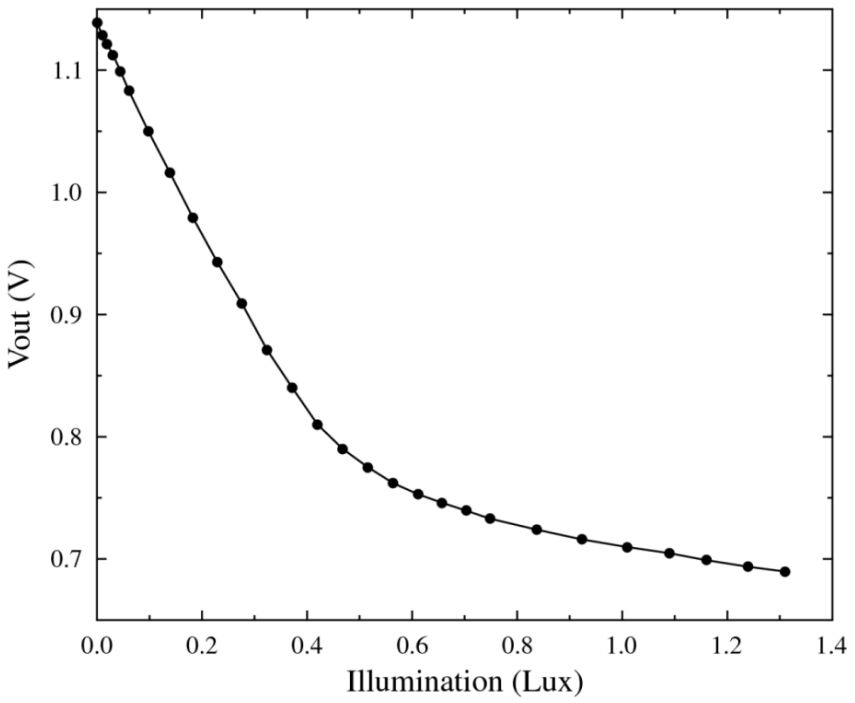
Results of Investigation



- Observe the operation of a pixel
  - a: reset
  - b: output (V_{ref}=2V)
- For this light intensity C_{MIM} fully discharged after 10ms.
- The unexpected behaviour is due to capacitive coupling between C_{MIM} and source follower input

Dual Slope Operation

- Opportunity to create a dual slope linear response
- V_{ref} controls the illumination at which the slope changes
- Test with V_{ref}=0.9V
- First slope is 0.78 V/lux
- Second slope 0.07 V/lux
- Result is increased dynamic range in comparison to linear mode



Conclusions

- A method of integrated wide dynamic range readout circuits between SPADs has been demonstrated
- A dual slope linear response has been obtained using a constant input reference voltage
- A wider dynamic range logarithmic response will be obtained when the input reference voltage is optimised for the circuit layout